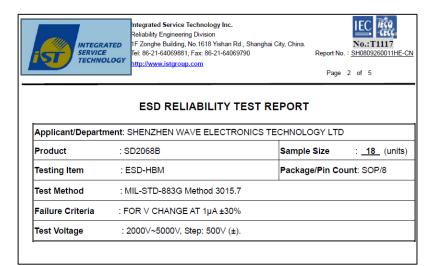
SD2068 可靠性测试/版权证书

1.ESD 测试报告:>5KV



ESD-HBM Testing Report

Test Equipment:

KEYTEK ZAPMASTER 7/4

Test Equipment S/N:

9608430

Calibration Date:

May 28, 2008

Recommended Due Date:

May 27, 2009

Environmental Condition of Laboratory:

Temperature: 25°C±5°C Humidity: 55%±10% RH

Test Condition:

IO VCC TO VSS (+)

10 VCC 10 VSS (-)

IO VSS TO VCC (+) IO VSS TO VCC (-)

IO TO IO (+)

IOTO IO (-)

Test Result:

MODEL: HBM	ESD SENSITIVITY PASS : ±5000V		V CLASS: 3
PIN COMBINATION	SAMPLE SIZE	PASSED VOLTS	NOTE:
IO VCC TO VSS (+)	3	+5000	FOR EIAJ TEST NO
IO VCC TO VSS (-)	3	-5000	CLASSIFICATION CLASS 0: < 250V
IO VSS TO VCC (+)	3	+5000	CLASS 1A: 250V TO 499V
IO VSS TO VCC (-)	3	-5000	CLASS 1B: 500V TO 999V CLASS 1C: 1000V TO 1999V
IO TO IO (+)	3	+5000	CLASS 2: 2000V TO 3999V
IOTO IO (-)	3	-5000	CLASS 3A: 4000V TO 7999V CLASS 3B: ≥ 8000V

VCC: Pin8; VSS: Pin4; IO: Pin1-3 5-7;

2. Latch up 电流 (>190mA):

REPORT FOR DEVICE: SD2068, Package: sop8 Latch-up: From 50mA to 190mA, step:20mA(+/-)

Sample No.

```
#L1, #L2, #L3: Positive Current Trigger: From +50mA to +190mA, step:20mA;
#L1, #L2, #L3: Negative Current Trigger: From -50mA to -190mA, step:20mA;
#L1, #L2, #L3: Vsupply Over voltage Test: From +5.0V to +8.0V, step:1V;
```

Pin Failure Column Label Explanations

```
SKT TESTPIN

LEVEL

#PULSES

APM. ZM

CVIM. CM

CRII

PVI | 11 | 12 | 12 |

Sec 2 (V1): for VS1 culrent, columns are mid- and post- pulse

Sec 3 (I1): for VS1 culrent, columns are mid- and post- pulse

Sec 4 (V2): for VS2 current, columns are mid- and post- pulse

Standard: JEDEC 78A

- Socket number of device for failed pin

- Mumber of Dulses applied to pin during most recent Zap Method

- Number of DurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of GurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of DurveTrace Method applied to pin

- Number of DurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of DurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of CurveTrace Method applied to pin

- Number of DurveTrace Method applied to pin

- Number of CurveTrace Method applied to pi
```

3. EFT 测试: (通过 4KV 的群脉冲(EFT)干扰)

- 。采用 IEC61000-4-4 标准
- 。实验设备:公司自有的 SANKI NS61000-4K
- 。试品板: 兴威帆的 SD2068 评估板(其电源采用变压器加三端稳压的方式,没有进行电磁的处理)
- 。测试方法: 试品板 AC 端接群脉冲发生器的输出端,分别在 AC 的 L、N 端加+4KV、-4KV 脉冲干扰群,检测时钟数据的变化。
- 。测试结果: 时钟数据没有复位、混乱的现象发生, 走时正常。

4.高温、低温测试: (通过高温+85℃、低温-40℃测试)

- 。试验设备:公司自有的高低温交变试验箱 GDJW-100(温度范围-40℃~+100℃)
- 。试品板: 兴威帆的 SD2068 老化板
- 。测试结果:在一40℃通电24小时和+85℃通电24小时的情况下,工作情况正常。

5.Rohs 报告:



Test Report

No. CANEC0803857101

Date: 21 Jul 2008

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SHENZHEN WAVE ELECTRONICS TECHNOLOGY LTD 3TH FLOOR,ANTONG BUILDING,MEIHUA ROAD,FUTIAN DISTRICT,SHENZHEN CHINA

The following sample(s) was/were submitted and identified on behalf of the clients as :

SD2068

SGS Job No. : 11169245 - SZ Date of Sample Received : 16 Jul 2008

Testing Period : 16 Jul 2008 - 21 Jul 2008

Test Requested : Selected test(s) as requested by client.

Test Method : Please refer to next page(s).

Test Results : Please refer to next page(s).

Conclusion : Based on the performed tests on submitted sample(s), the results comply

with the RoHS Directive 2002/95/EC and its subsequent amendments.

6.版权证书



布图设计登记号: BS. 07500394. 5

布图设计申请日: 2007年12月7日

布图设计权利人姓名或名称: 深圳市兴威帆电子技术有限公

司

布图设计权利人地址:深圳市福田区梅华路 207 号安通大厦

三楼东

布图设计名称: SD2068A

布图设计的创作完成日: 2007年7月3日 布图设计首次投入商业利用日: 2007年11月1日

布图设计有次投入商业利用日: 2007年11月1

布图设计领证日: 2008年2月21日

登记证书号



根据集成电路布图设计保护条例第十八条规定,本布图 设计登记申请,经初步审查,未发现驳回理由,予以登记, 发给此登记证书,并予以公告。

根据集成电路布图设计保护条例实施细则第二十条规

定,本布图设计专有权自申请日起生效。

第 1621 号

根据集成电路布图设计保护条例第十二条规定,布图设计专有权的保护期为 10 年,自布图设计登记申请之目或者 在世界任何地方首次投入商业利用之日起计算,以较前日期 为准,但是,无论是否登记或者投入商业利州,布图设计自 创作完成之日起15 年后,不再受该条例保护,

易长 切力夢



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